which are to be tested. This is stated at the beginning of the Gheewala specification. "Modern integrated circuits (IC's) contain a large number of components or elements, most of which can be classified as either storage elements (i.e., a type of memory element such as a latch or flip-flop) or gates (i.e., non-memory such as combinational logic gate, invertors, and the like). In the process of designing and manufacturing integrated circuits, it is desired to test integrated circuits to determine whether the components of the integrated circuit are operating in the desired fashion (underlining added for emphasis)." Col. 1, lines 13-21. Most of the description of this reference describes the testing of storage elements 112 (see, e.g., col. 3, lines 15-16), in the form of data latches 132 (see, e.g., col 3, lines 55-59). It is these storage elements which are referred to in the first sentence of the Abstract. However, the applicants' independent claims 1 and 10 call for storage elements which comprise the probe lines which in turn carry system operation signals from predetermined probe points.

To test these storage elements, i.e., the data latches 132, Gheewala connects the data latches to probe lines 124 and select lines 122. See the description in terms of storage elements, col. 3, lines 26-32, or in terms of data latches, col. 3, lines 55-59. Details of Gheewala's probe lines and storage elements are revealed by a close inspection of Fig. 4, which is the cover drawing of the Gheewala '486 patent. A probe line (PLm) 124 is connected to the gate electrodes of the transistors of the transmission gate 138 (T3), the input terminal of the inverter 140 (G4), and the gate electrode of the transistor 134. Control signals are carried to the storage element, data latch 132. It is evident from this circuit arrangement that data signals cannot be carried from the data latch 132 on the probe line 124. This is consistent with Table I in which there are only input signals on probe line Pl_m and no output signals, termed RESULTS, on the probe line. Furthermore, it should be noted the applicants have amended claims 1 and 10 so that they now recite that "said probe lines comprise strings of storage elements providing signal paths from said probe points to said memory (or unit)." This is the applicants' second point.

Finally, even assuming for argument's sake, that the select lines of Gheewala are to be analogized to the applicants' probe lines, this analogy does not meet the language of the applicants' claims either. In his Summary of the Invention Gheewala states, "Data which is placed on one of the select lines can be directly (i.e., without intervening storage in another

storage element of the main circuitry of the IC) stored in one of the latches. Data stored in one of the latches can be output to the associated select line for direct observation (i.e., without subsequent storage in another storage element of the main circuitry of the IC)." Col 2, lines 48-54. On the other hand, claim 1 recites, "...a plurality of probe lines responsive to said control unit for carrying system operation signals from predetermined probe points of said logic blocks, wherein said probe lines comprise strings of storage elements providing signal paths from said probe points to said memory, said signal paths capable of moving sets of said system operation signals at system operation clock rates...." The claimed probe lines comprise strings of storage elements providing signal paths from said probe points. In Gheewala's terminology, the applicants have intervening storage and no direct observation.

Additionally, there are technical reasons why Gheewala's sense lines cannot be analogized to the applicants' probe lines which are recited as being capable of moving sets of said system operation signals at system operation clock rates. The select lines are driven from the ARWC (addressing and read/write control component) 126 in Fig. 3 and the transistor 134 in Fig. 4. As a result, many loads (134s) are connected in PARALLEL on a single sense line 122. This is a condition more accurately represented by the CCL in Fig. 5, which is sensed via sense line 122b and probed via probe line 124c. Therefore the performance-limiting capacitance argument already presented in the July 5, 2001 amendment applies here as well. Gheewala does not teach a serial path for the transfer of data, as implied by the phrase, "string of storage elements," in applicants' claims 1 and 10.

In summary, the Gheewala '486 patent neither by itself nor in combination with other previously cited references does not render the applicants' claimed invention unpatentable. Claims 1 and 10 are patentable and claims 2-9 and 11-14 which are dependent upon these independent claims are also patentable.

The applicants have also amended claim 15 to better distinguish their invention over the presently discussed Gheewala patent and the other references previously cited. Claim 15 and dependent claims 16-22 should also be patentable.

Therefore, in view of the amendments above and remarks thereto, the applicants respectfully request that the rejections be removed, that claims 1-22 be allowed and the case be passed to issue.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at (650) 564-9888.

Respectfully submitted,

Gary T. Aka
Reg. No. 29,038
Attorney for Applicants

LAW OFFICES OF GARY T. AKA
12930 Saratoga Avenue, Suite D1
Saratoga, California 95070
Tel: (650) 564-9888
Fax: (650) 564-9889
GTA:hs